

## **ABSTRACT OF THE DISCLOSURE**

A buffer circuit for a liquid crystal display device that comprises a first transistor further comprising a gate connectable to an input signal, a first electrode coupled to a first power supply, and a second electrode connectable to a second power supply, a second transistor further comprising a gate coupled to the second electrode of the first transistor, a first electrode connectable to the first power supply, and a second electrode connectable to the second power supply, a first capacitor being connectable to the input signal storing a voltage of the input signal when connected to the input signal, and providing a first voltage to the gate of the first transistor when disconnected from the input signal, a second capacitor further comprising a terminal coupled to the second electrode of the first transistor and the gate of the second transistor providing a second voltage at the terminal when the first transistor is turned on, and a third capacitor coupled to the first electrode of the second transistor providing a third voltage when the second transistor is turned on, wherein the second voltage further comprises a first offset including a gate to source voltage of the first transistor, and the third voltage further comprises a second offset including a gate to source voltage of the second transistor.

FINNEGAN  
HENDERSON  
FARABOW  
GARRETT &  
DUNNER LLP

1300 I Street, NW  
Washington, DC 20005  
202.408.4000  
Fax 202.408.4400  
[www.finnegan.com](http://www.finnegan.com)